

ABSTRACT

A method of fabricating a semiconductor device including providing a semiconductor heterostructure, the heterostructure having a relaxed $\text{Si}_{1-x}\text{Ge}_x$ layer on a substrate, a strained channel layer on the relaxed $\text{Si}_{1-x}\text{Ge}_x$ layer, and a $\text{Si}_{1-y}\text{Ge}_y$ layer; removing the $\text{Si}_{1-y}\text{Ge}_y$ layer; 5 and providing a dielectric layer. The dielectric layer includes a gate dielectric of a MISFET. In alternative embodiments, the heterostructure includes a SiGe spacer layer and a Si layer.